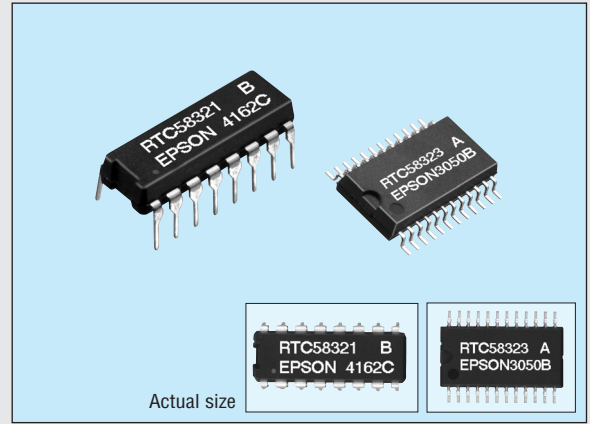


4-bit I/O CONNECTION REAL TIME CLOCK MODULE

# RTC-58321/58323

- Built-in crystal unit allows adjustment-free efficient operation.
- Incorporating time counter (hour, minute, sec.) and calendar counter (year, month, day of week).
- Either 12 h or 24 h selectable and leap year automatically adjustable.
- Standard signal output selectable among a choice of 1024 Hz, 1 sec., 60 sec., and 1 hour.
- Provided with counter start, stop and reset functions.
- Data transmission is by 4-bit bidirectional bus line and memory read and write method.
- Low current consumption and backup function provided.



## Specifications (characteristics)

### Absolute Max. rating

Item	Symbol	Condition	Specifications	Unit
Power source voltage	V <sub>DD</sub>	T <sub>a</sub> =+25 °C	-0.3 to 6.5	V
Input and output voltage	V <sub>I/O</sub>		-0.3 to V <sub>DD</sub> +0.3	
storage temperature	T <sub>STG</sub>	—	-55 to +85	°C
Soldering condition	T <sub>SOL</sub>	RTC-58321	Under +260 °C within 10 s (lead part) (package should be less than +150 °C)	
		RTC-58323	Twice at under +260 °C within 10 s or under +230 °C within 3 min.	

### Operating range

Item	Symbol	Condition	Specifications	Unit
Operating voltage	V <sub>DD</sub>	—	4.5 to 5.5	V
Operating temperature	T <sub>OPR</sub>	RTC-58321	-10 to +70	°C
		RTC-58323	-30 to +85	
Data holding voltage	V <sub>DH</sub>	—	2.2 to 5.5	V
CSI data holding time	t <sub>CDR</sub>	Refer to the data holding timing	0 Min.	µs
Operation restoring time	t <sub>r</sub>			

### Frequency characteristics and current consumption characteristics

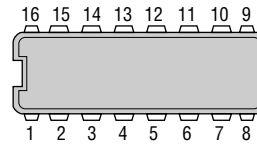
Item	Symbol	Condition	Specifications	Unit	
Frequency tolerance	Δf/fo	T <sub>a</sub> =+25 °C V <sub>DD</sub> =5 V	58321 A	±10	
			58321 B		±50
			58323		5±20
Frequency temperature characteristics	—	-10 °C to +70 °C (+25 °C reference temperature)	+10/-120		
Aging	f <sub>a</sub>	V <sub>DD</sub> =5 V, T <sub>a</sub> =+25 °C, first year	±5 Max.	x 10 <sup>3</sup> /year	
Shock resistance	S.R.	Three drops on a hard board from 750 mm or 29400 m/s <sup>2</sup> x 0.3 ms x 1/2 sine wave x 3 directions	±10 Max.	x 10 <sup>6</sup>	
Current consumption	I <sub>DD1</sub>	V <sub>DD</sub> =5 V, CS <sub>1</sub> =0 V	40 Max.	µA	
	I <sub>DD2</sub>	V <sub>DD</sub> =3 V, CS <sub>1</sub> =0 V	20 Max.		

### DC characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable terminal
"H" input voltage	V <sub>IH1</sub>	—	3.6	—	—	V	Input other than CS <sub>1</sub>
"H" input voltage	V <sub>IH2</sub>		V <sub>DD</sub> -0.5	—	—		
"L" input voltage	V <sub>IL</sub>	—	—	—	0.8		
"L" output voltage	V <sub>OL</sub>		I <sub>OL</sub> =1.6 mA	—	—		
"L" output current	I <sub>OL</sub>	V <sub>O</sub> =0.4 V	1.6	—	—	mA	
"H" input current	I <sub>IH</sub>	V <sub>I</sub> =5 V	10	30	80	µA	Input other than D <sub>0</sub> to D <sub>3</sub>
"L" input current	I <sub>IL</sub>	V <sub>I</sub> =0 V	—	—	-1		
Input leak current	I <sub>L1H</sub>	V <sub>I</sub> =5 V	—	—	1	µA	D <sub>0</sub> to D <sub>3</sub>
Input off leak current	I <sub>L1L</sub>	V <sub>I</sub> =0 V	—	—	-1		
Input capacity	C <sub>I</sub>	Input frequency 1 MHz	—	5	—	pF	
Oscillation start-up time	t <sub>OSC</sub>	V <sub>DD</sub> =5 V T <sub>a</sub> =+25 °C	1.5	3.0	—	s	Busy output

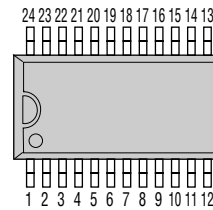
### Terminal connection

#### RTC-58321



No.	58321	No.	58323
1	CS <sub>2</sub>	1 to 4	N.C
2	WRITE	5	CS <sub>2</sub>
3	READ	6	WRITE
4	D <sub>0</sub>	7	READ
5	D <sub>1</sub>	8	D <sub>0</sub>
6	D <sub>2</sub>	9	D <sub>1</sub>
7	D <sub>3</sub>	10	D <sub>2</sub>
8	GND	11	D <sub>3</sub>
9	ADDRESS WRITE	12	GND
10	BUSY	13	ADDRESS WRITE
11	STOP	14	BUSY
12	TEST	15	STOP
13	CS <sub>1</sub>	16	TEST
14 to 15	N.C	17	CS <sub>1</sub>
16	V <sub>DD</sub>	18 to 24	V <sub>DD</sub>

#### RTC-58323

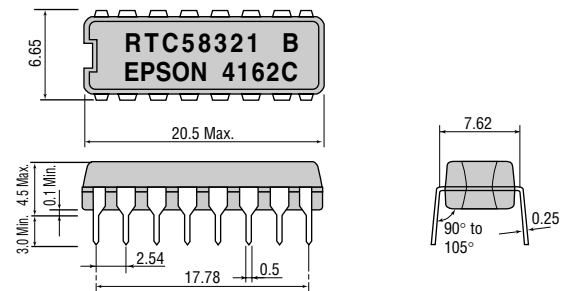


● NC is not connected internally.

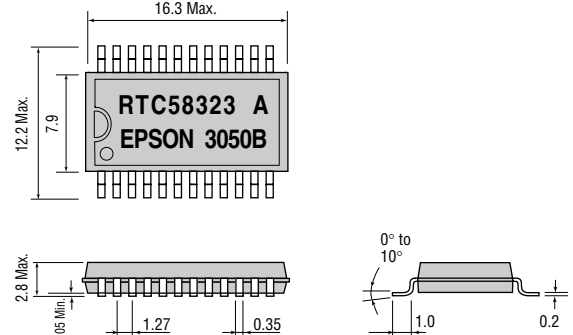
### External dimensions

(Unit: mm)

#### RTC-58321



#### RTC-58323



Supplement

0= "L" level 1= "H" level

Item	Description																									
* mark	Writable. Recognized as 0 while in read mode																									
24/12	"1" =24 h mode, "0" =12 h mode																									
PM/AM	"1" =PM, "0" =AM. In 24 h mode, this will be "0"																									
D <sub>3</sub> and D <sub>2</sub> of 10 days digit	Used to select leap year. Calculated according to the surplus after dividing 10 year digit by 4 <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Calendar</th> <th>D<sub>3</sub></th> <th>D<sub>2</sub></th> <th>Surplus after dividing 10 year digit by 4</th> <th>Example of leap year</th> </tr> </thead> <tbody> <tr> <td>Gregorian calendar</td> <td>0</td> <td>0</td> <td>0</td> <td>96, 00</td> </tr> <tr> <td></td> <td>1</td> <td>1</td> <td>3</td> <td></td> </tr> <tr> <td>Spare</td> <td>1</td> <td>0</td> <td>2</td> <td></td> </tr> <tr> <td></td> <td>1</td> <td>1</td> <td>1</td> <td></td> </tr> </tbody> </table>	Calendar	D <sub>3</sub>	D <sub>2</sub>	Surplus after dividing 10 year digit by 4	Example of leap year	Gregorian calendar	0	0	0	96, 00		1	1	3		Spare	1	0	2			1	1	1	
Calendar	D <sub>3</sub>	D <sub>2</sub>	Surplus after dividing 10 year digit by 4	Example of leap year																						
Gregorian calendar	0	0	0	96, 00																						
	1	1	3																							
Spare	1	0	2																							
	1	1	1																							
Reset register	These selections are for resetting 5-stage and the busy circuit after 1/2 <sup>5</sup> frequency stage. Resetting is activated by latching this code on to the address latch and setting WRITE=H																									
Standard signal register	By latching this code to the address latch and setting READ to H, the standard signals will be output at D <sub>0</sub> to D <sub>3</sub>																									

- Note:
- Do not enter erroneous data for clock.
  - This may result in time keeping error.
  - Do not change STOP more than once while in BUSY mode.

Switching characteristics

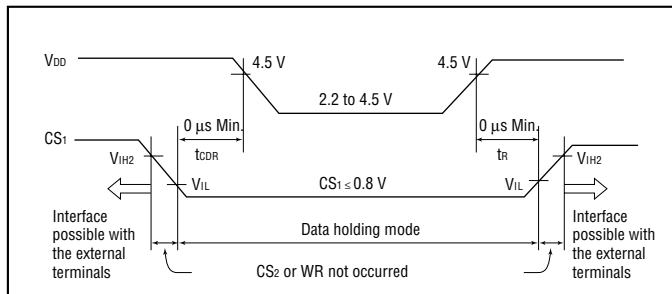
Write & read mode

(V<sub>DD</sub>=5 V±0.5 V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit.
CS setup time	t <sub>CS</sub>	—	0	—	—	μs
Address setup time	t <sub>AS</sub>		0.5			
Address write pulse width	t <sub>AW</sub>		0.1			
Address hold time	t <sub>AH</sub>		0			
Data setup time	t <sub>DS</sub>		2			
Write pulse width	t <sub>WW</sub>		0			
Data hold time	t <sub>DH</sub>		—			
Read inhibit time	t <sub>RI</sub>		—			
Read access time	t <sub>RA</sub>		—			
Read delay time	t <sub>DD</sub>		—			
CS hold time	t <sub>CH</sub>	0	—			

\*1 t<sub>RA</sub>=1 μs+C x R x ln [V<sub>DD</sub>/(V<sub>DD</sub>-V<sub>H</sub>)]  
 C: Data line capacity  
 R: Pull-up resistance  
 V<sub>H</sub>: "H" input voltage connected to the data line  
 ln: Natural logarithm

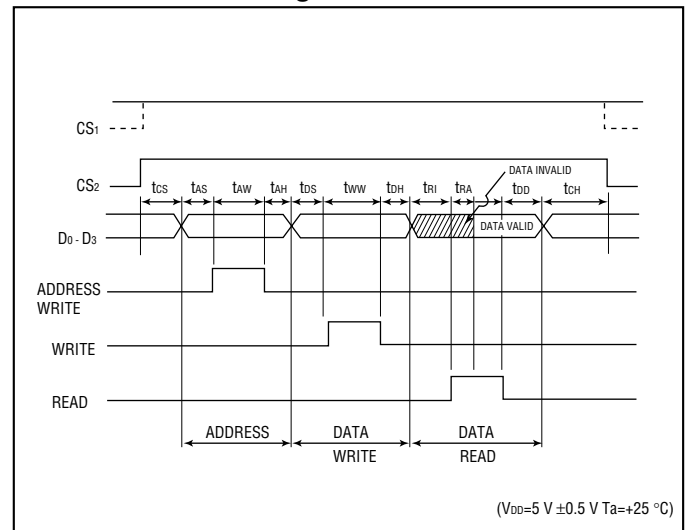
Date holding timing



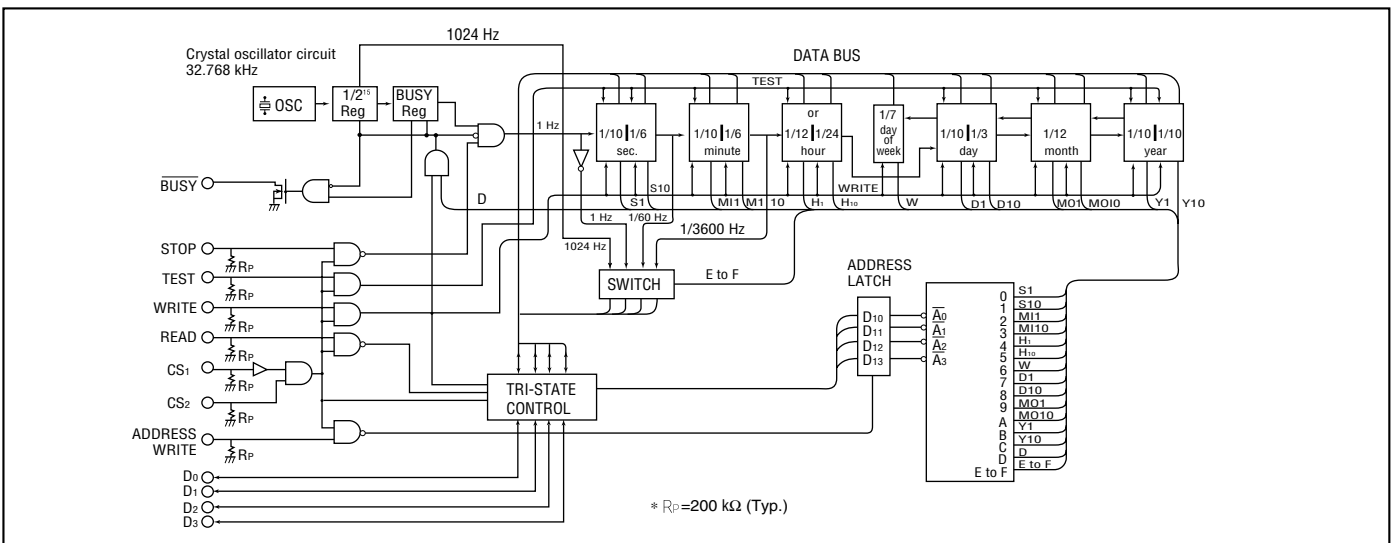
Register table

Address	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	Name of register	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	Count	Note	
	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		S <sub>8</sub>	S <sub>4</sub>	S <sub>2</sub>	S <sub>1</sub>			
0	0	0	0	0	S <sub>1</sub>	S <sub>8</sub>	S <sub>4</sub>	S <sub>2</sub>	S <sub>1</sub>	0 to 9	1 - sec. digit register	
1	0	0	0	1	S <sub>10</sub>	*	S <sub>40</sub>	S <sub>20</sub>	S <sub>10</sub>	0 to 5	10 - sec. digit register	
2	0	0	1	0	M <sub>1</sub>	mi <sub>8</sub>	mi <sub>4</sub>	mi <sub>2</sub>	mi <sub>1</sub>	0 to 9	1 - min. digit register	
3	0	0	1	1	M <sub>10</sub>	*	mi <sub>40</sub>	mi <sub>20</sub>	mi <sub>10</sub>	0 to 5	10 - min. digit register	
4	0	1	0	0	H <sub>1</sub>	h <sub>8</sub>	h <sub>4</sub>	h <sub>2</sub>	h <sub>1</sub>	0 to 9	1 - hour digit register	
5	0	1	0	1	H <sub>10</sub>	24/12	PM/AM	h <sub>20</sub>	h <sub>10</sub>	0 to 2 or 0 to 1	10 - hour digit register	
6	0	1	1	0	W	*	W <sub>4</sub>	W <sub>2</sub>	W <sub>1</sub>	0 to 6	Week register	
7	0	1	1	1	D <sub>1</sub>	d <sub>8</sub>	d <sub>4</sub>	d <sub>2</sub>	d <sub>1</sub>	0 to 9	1 - day digit register	
8	1	0	0	0	D <sub>10</sub>	Leap year selection			d <sub>20</sub>	d <sub>10</sub>	0 to 3	10 - day digit register
9	1	0	0	1	M <sub>0</sub>	mo <sub>8</sub>	mo <sub>4</sub>	mo <sub>2</sub>	mo <sub>1</sub>	0 to 9	1 - month digit register	
A	1	0	1	0	M <sub>0</sub>	*			mo <sub>10</sub>	0 to 1	10 - month digit register	
B	1	0	1	1	Y <sub>1</sub>	y <sub>8</sub>	y <sub>4</sub>	y <sub>2</sub>	y <sub>1</sub>	0 to 9	1 - year digit register	
C	1	1	0	0	Y <sub>10</sub>	y <sub>80</sub>	y <sub>40</sub>	y <sub>20</sub>	y <sub>10</sub>		10 - year digit register	
D	1	1	0	1	—	*					Reset register	
E	1	1	1	0	—	1 hour	1 min.	1 sec.	1024 Hz		Standard signal register	
F	1	1	1	1	—							

Write and read timing



Block diagram



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